

Figure 1

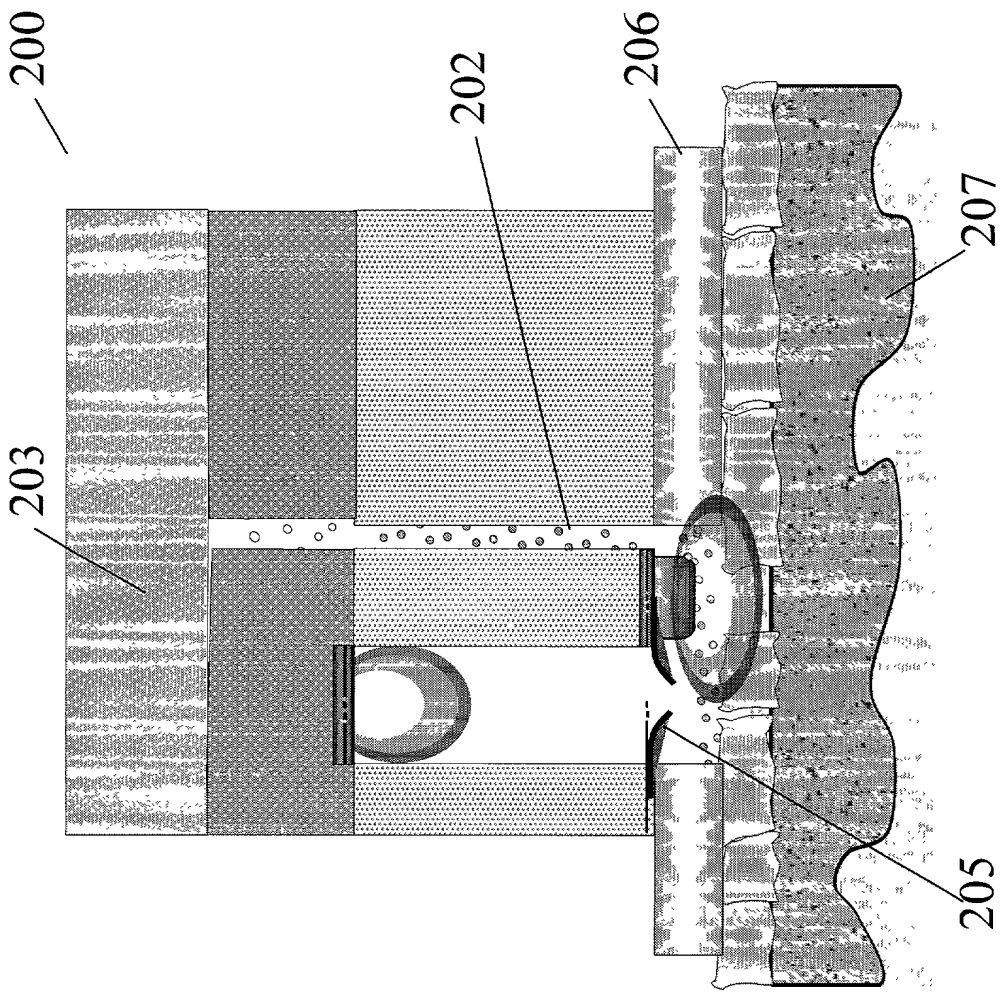


Figure 2

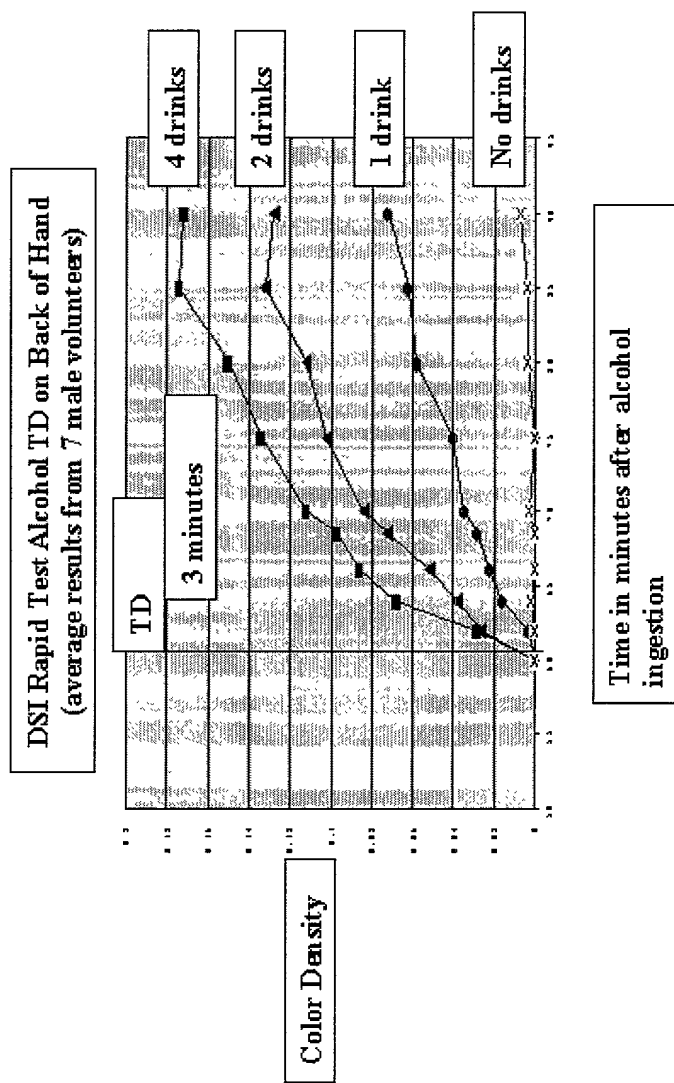


Figure 3

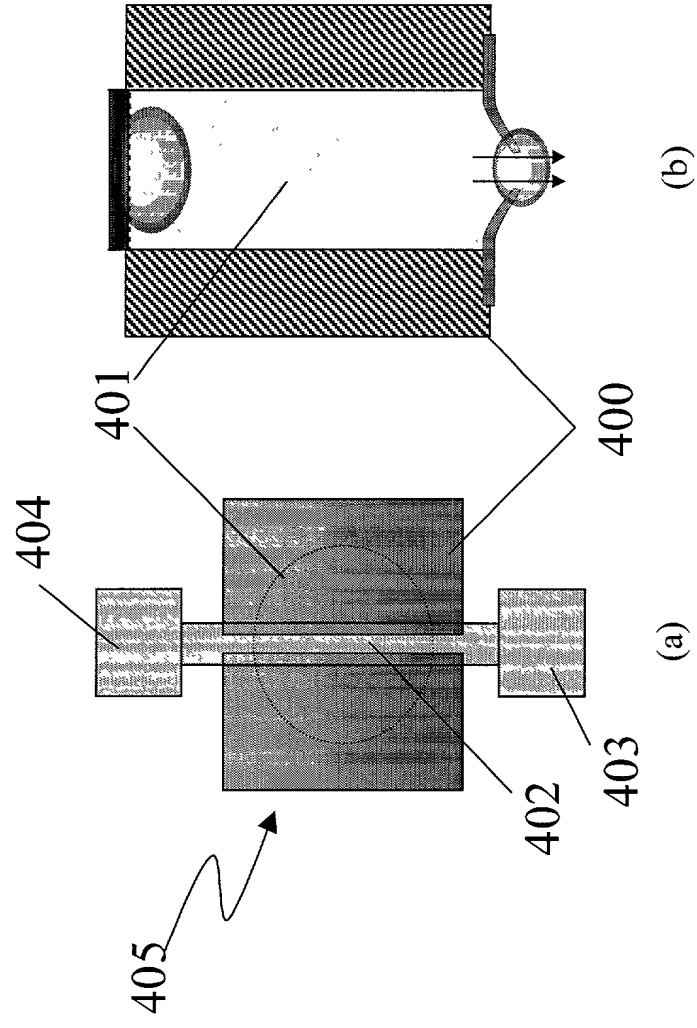


Figure 4

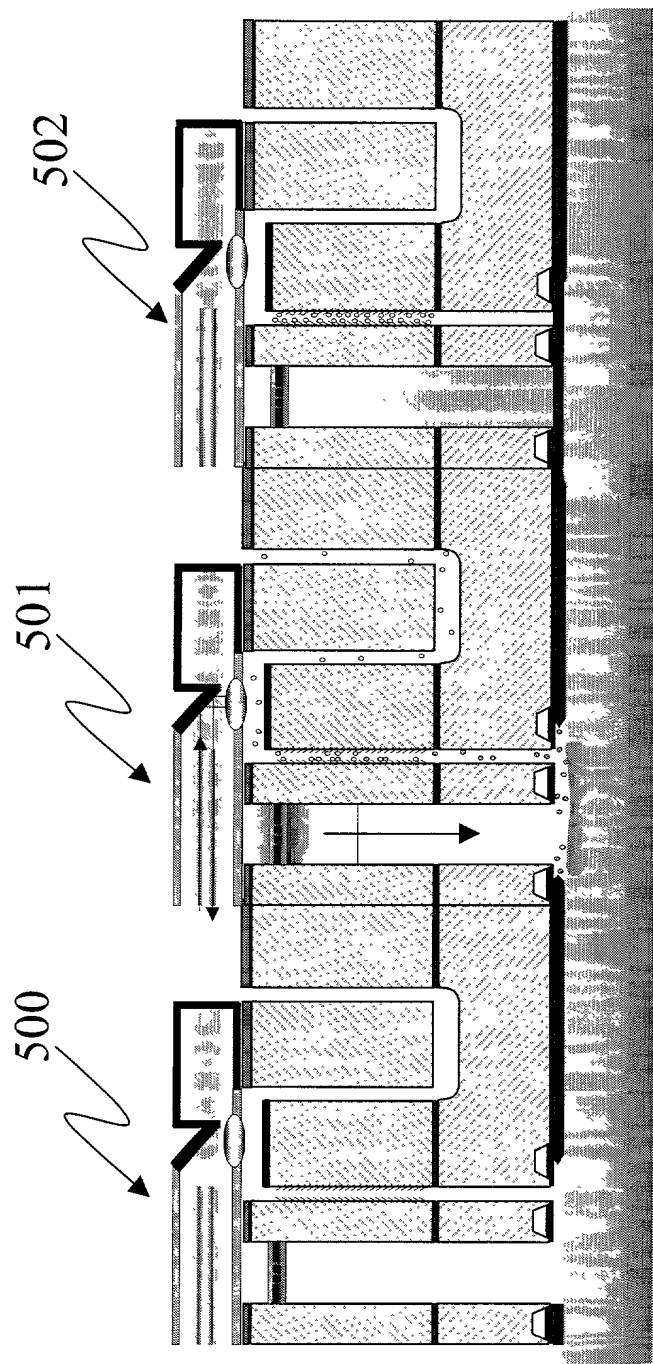


Figure 5

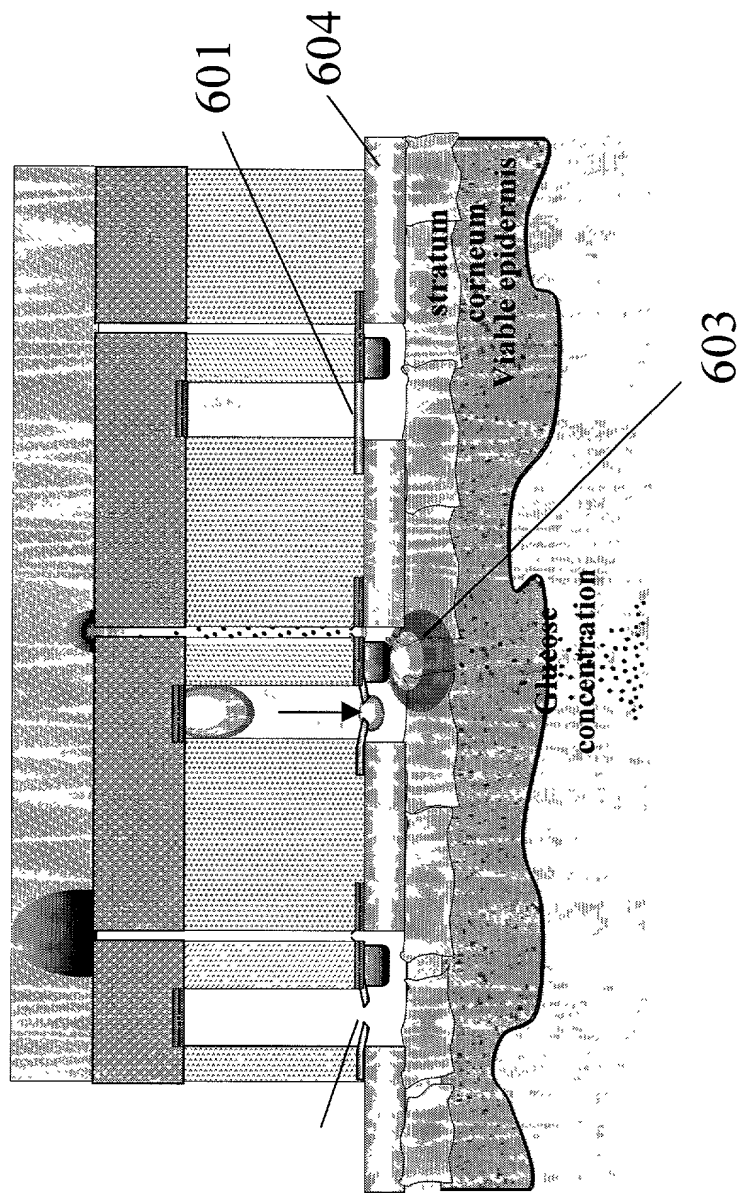


Figure 6

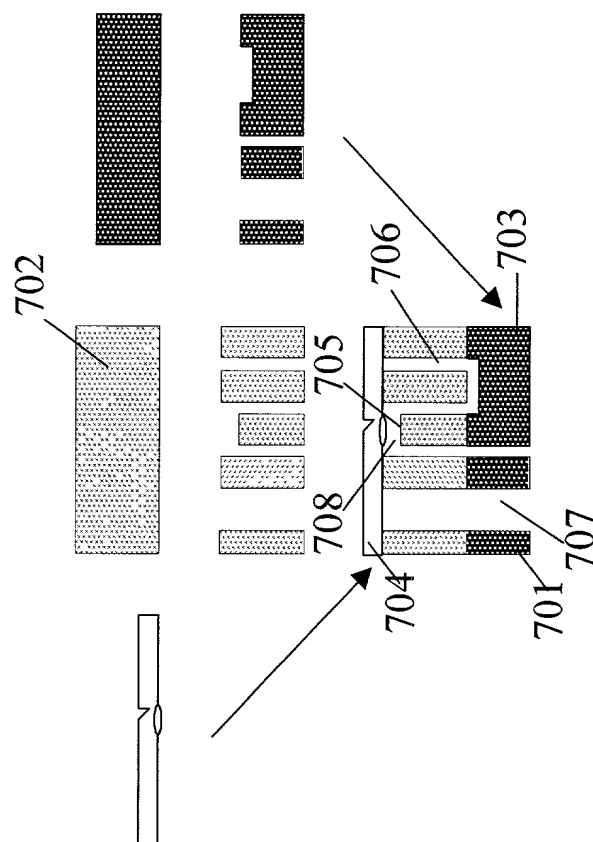


Figure 7

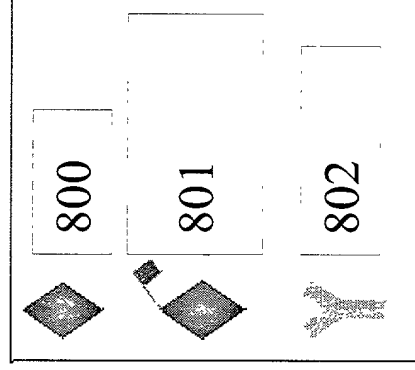
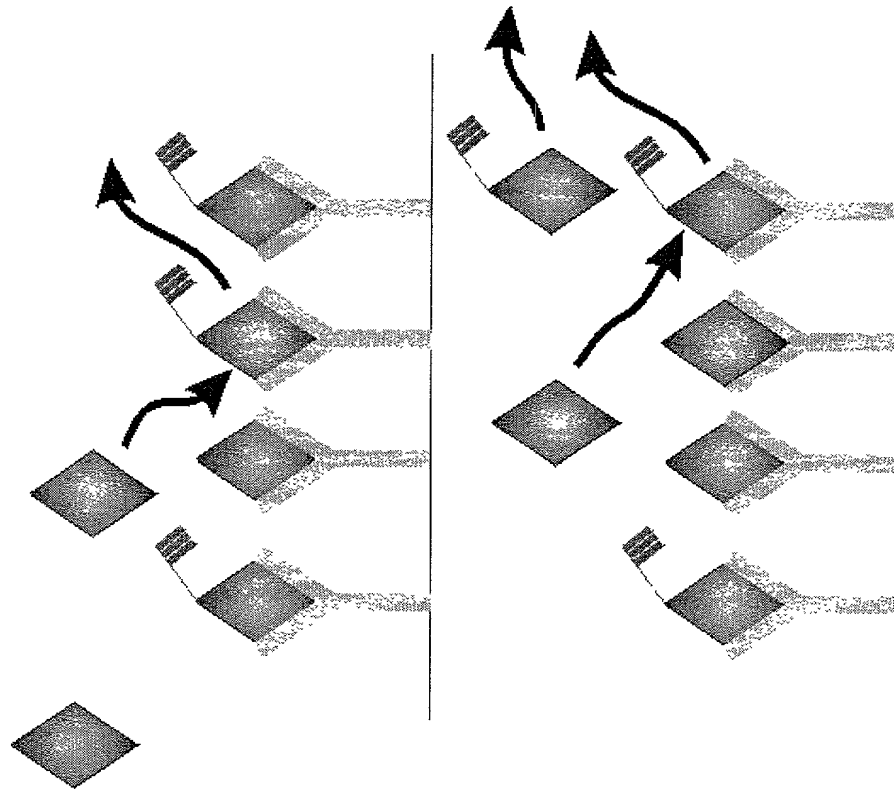


Figure 8

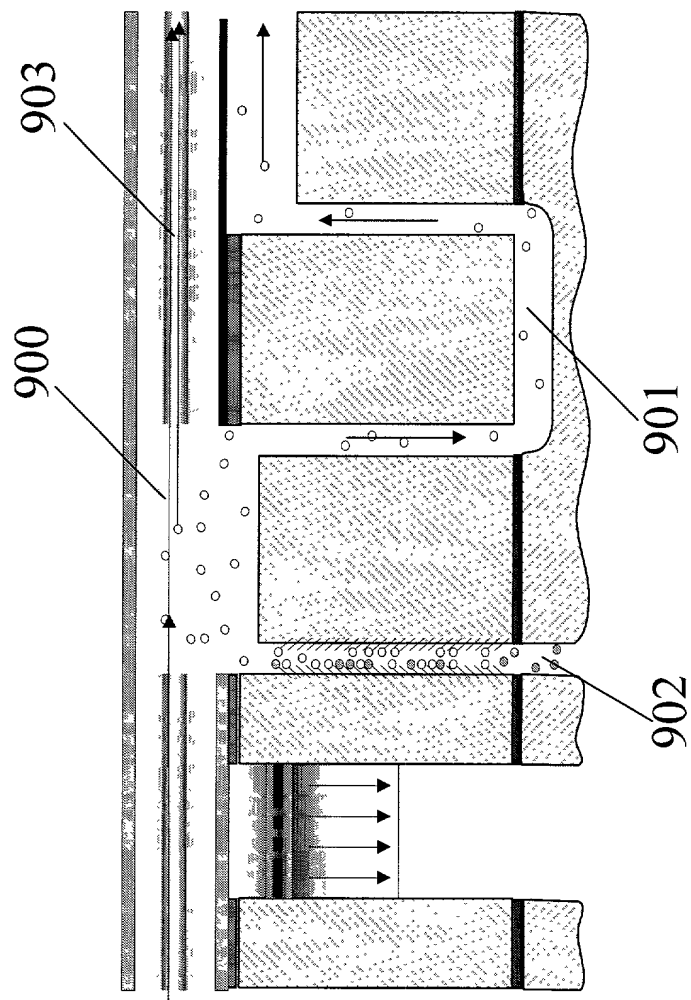


Figure 9

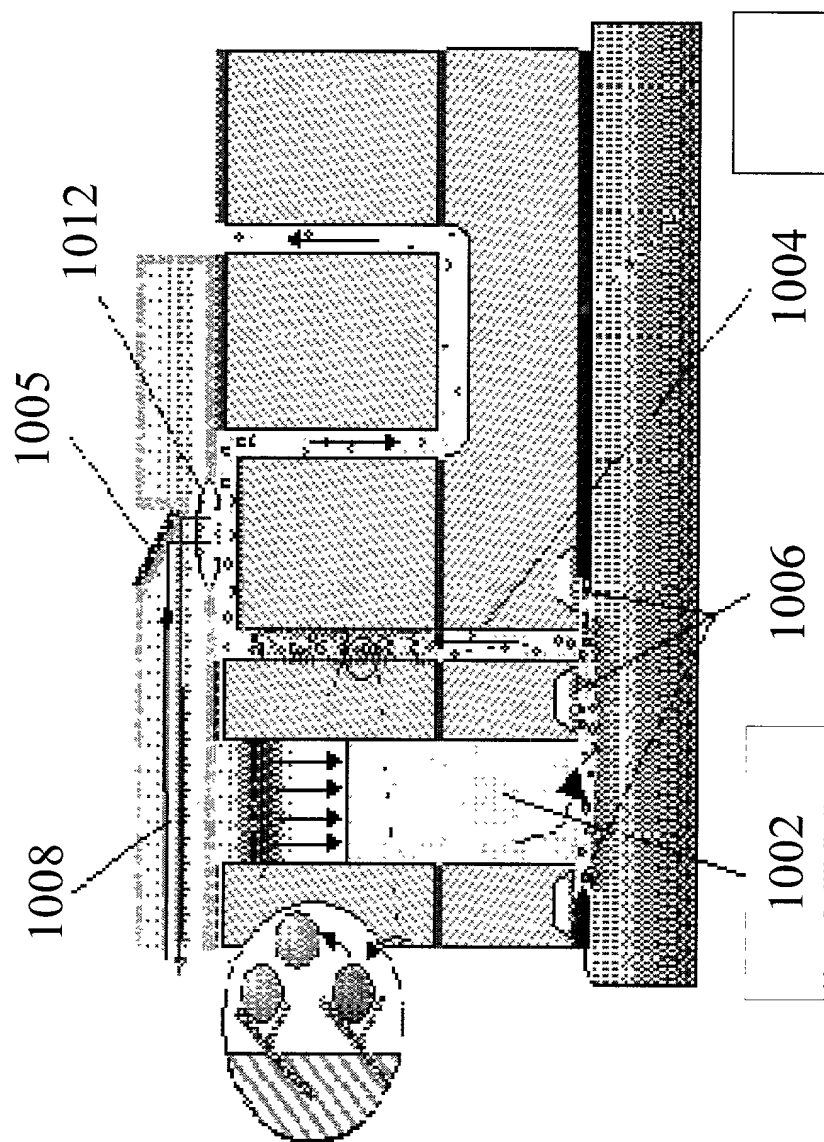


Figure 10

FIG. 11 is a cross-sectional view of a device 1100, showing a substrate 1102, a gate stack 1104, a gate electrode 1106, a channel layer 1108, a source/drain region 1110, a source/drain contact 1112, a source/drain pad 1114, and a source/drain pad 1116.

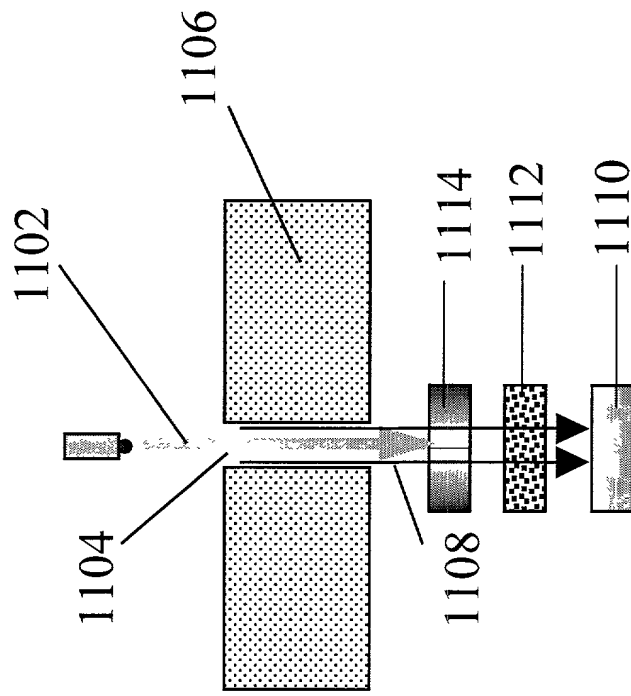


Figure 11

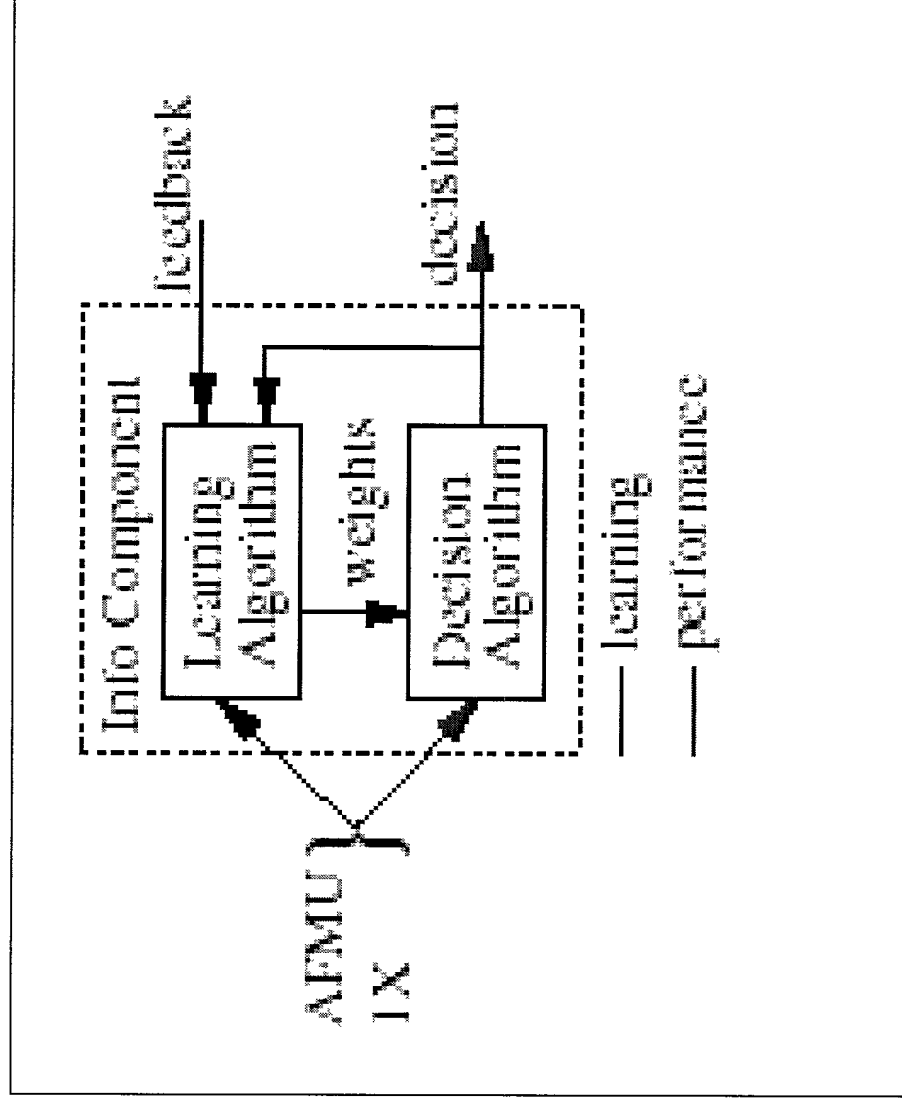


Figure 12

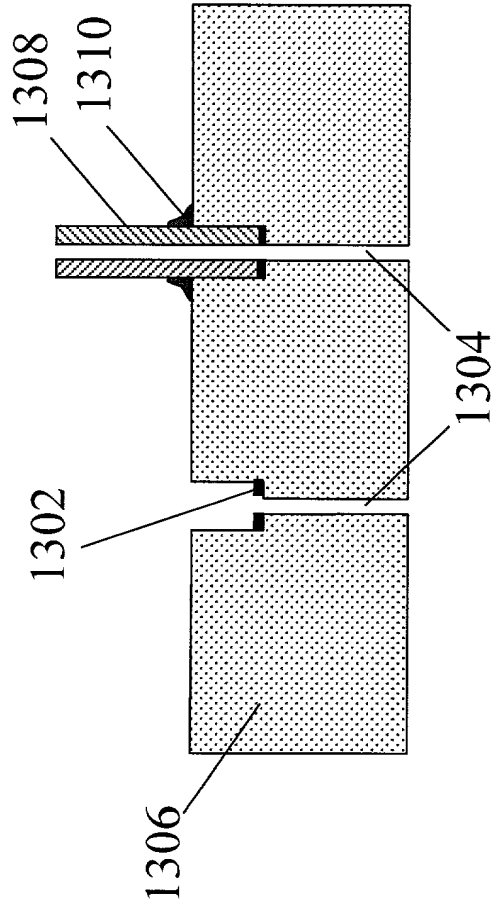


Figure 13

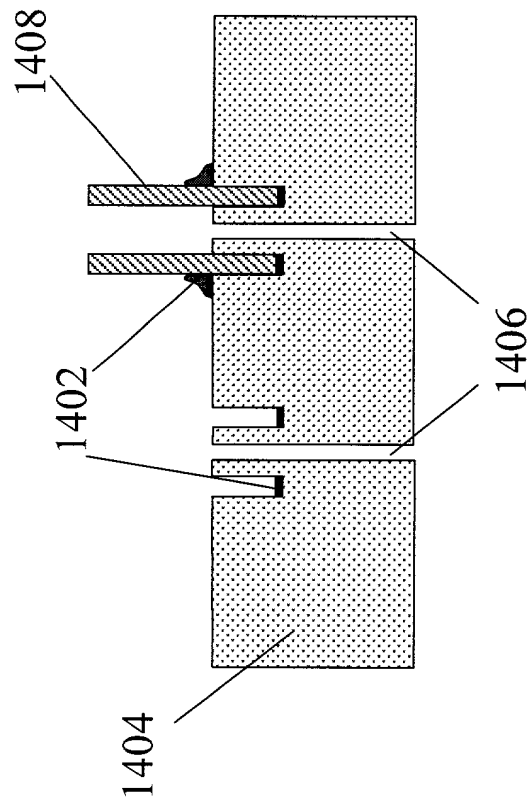


Figure 14

FIG. 15 is a schematic diagram of a device 1500, which may be a display device, a lighting device, or a combination thereof. The device 1500 includes a substrate 1502, a first layer 1504, a second layer 1506, a third layer 1508, and a fourth layer 1510. The first layer 1504 is a substrate, the second layer 1506 is a buffer layer, the third layer 1508 is an active layer, and the fourth layer 1510 is a capping layer. The device 1500 is configured to emit light through the first layer 1504.

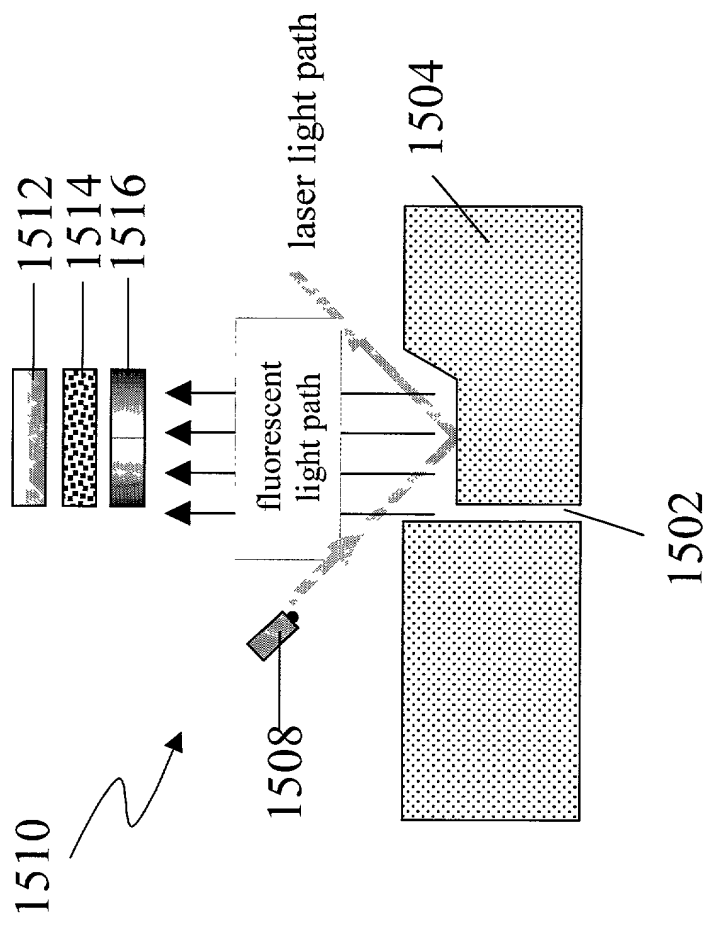


Figure 15

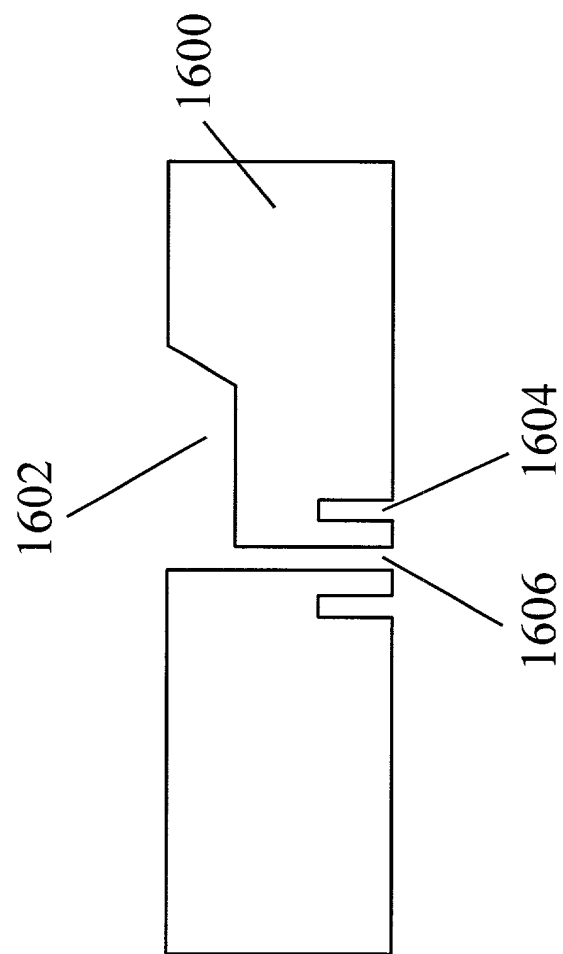


Figure 16

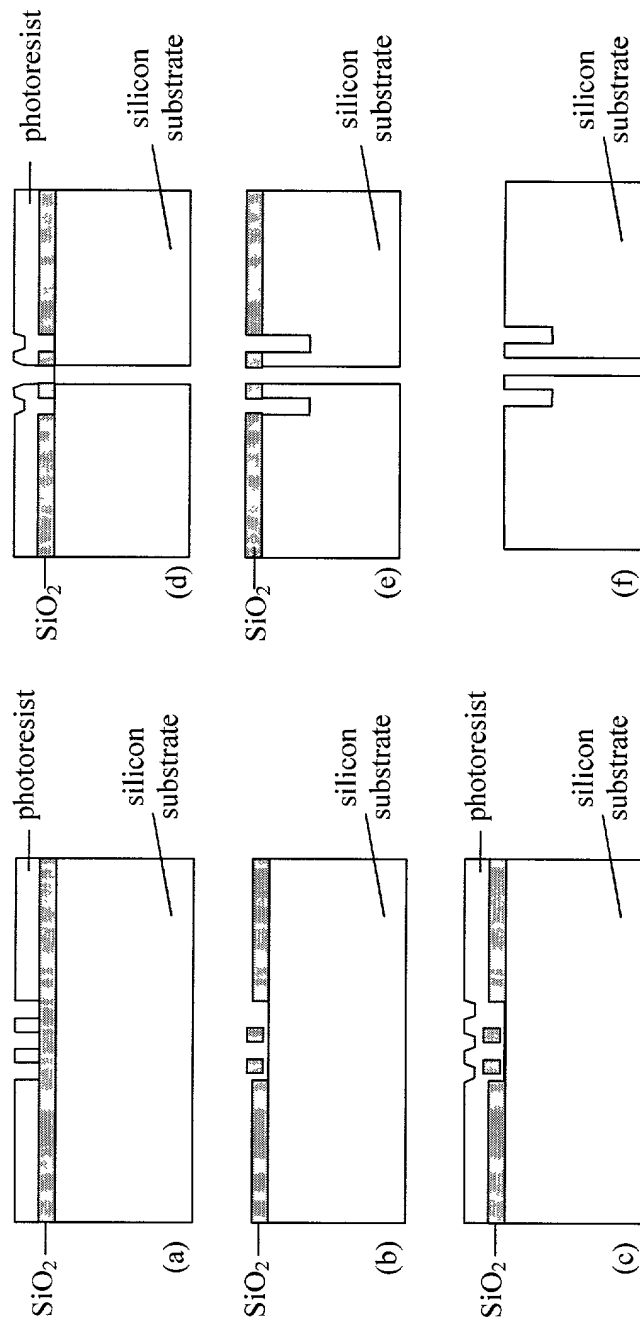


Figure 17

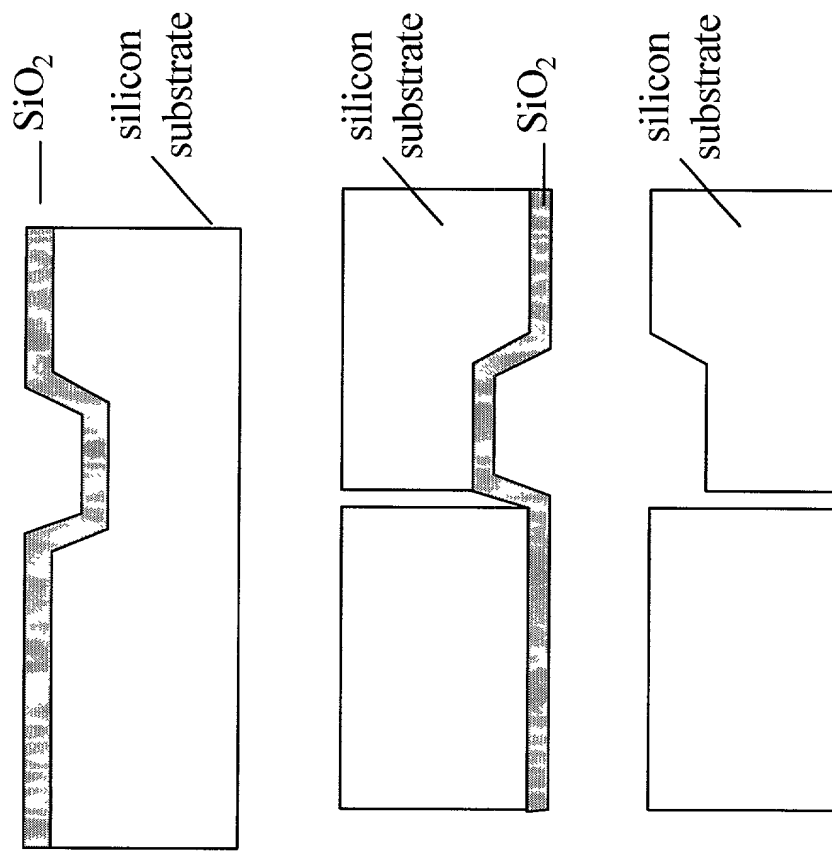


Figure 18

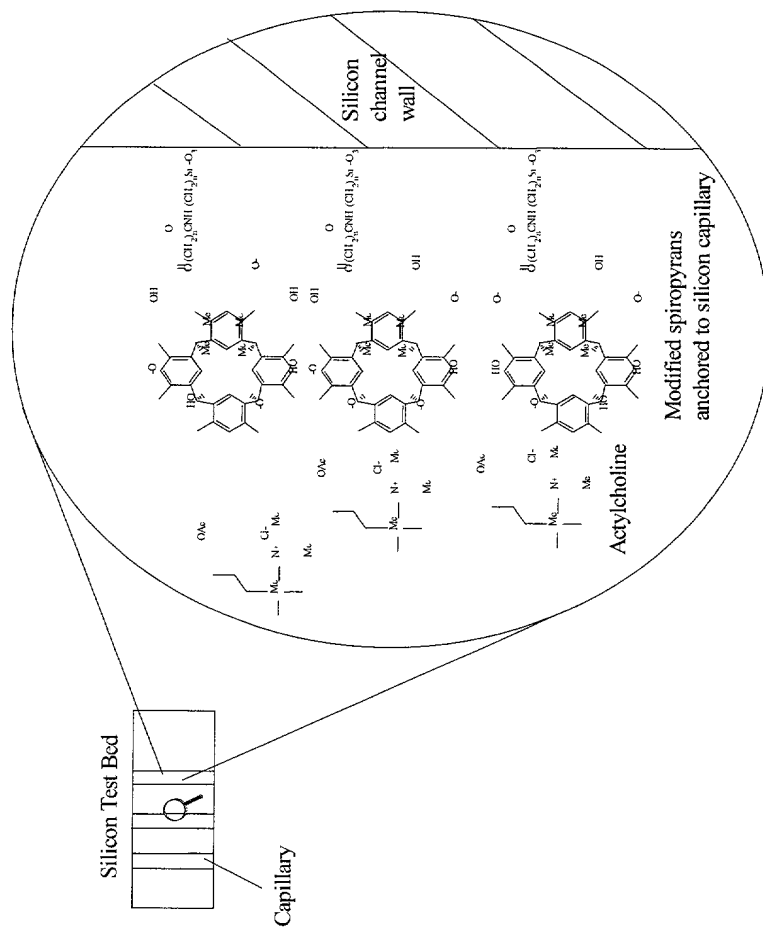


Figure 19

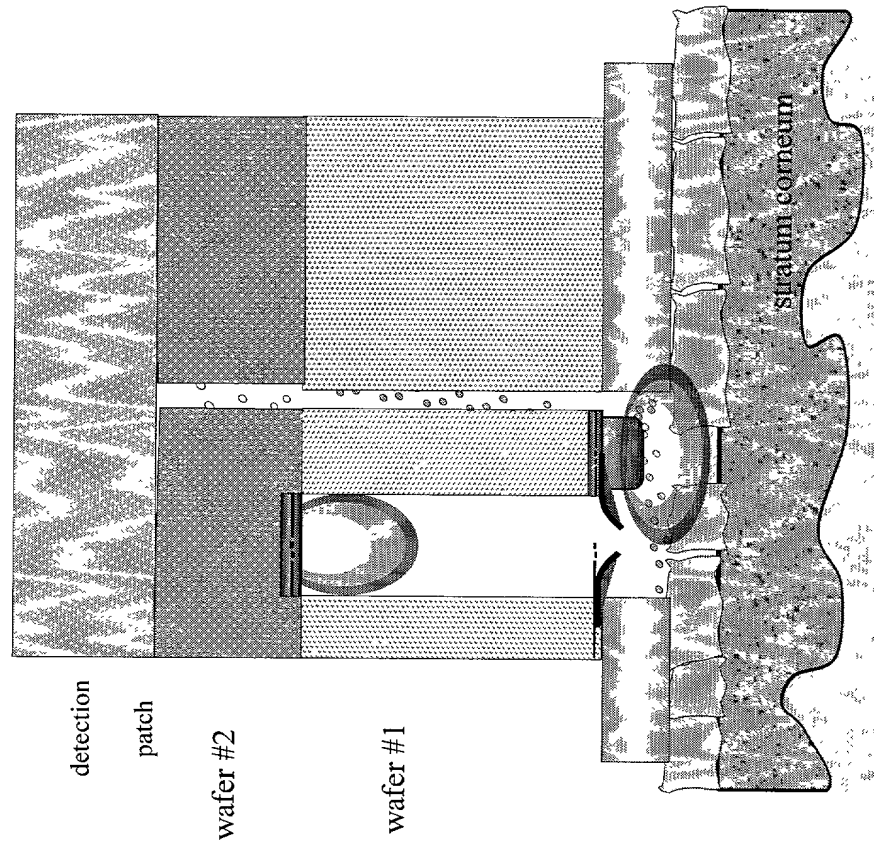


Figure 20

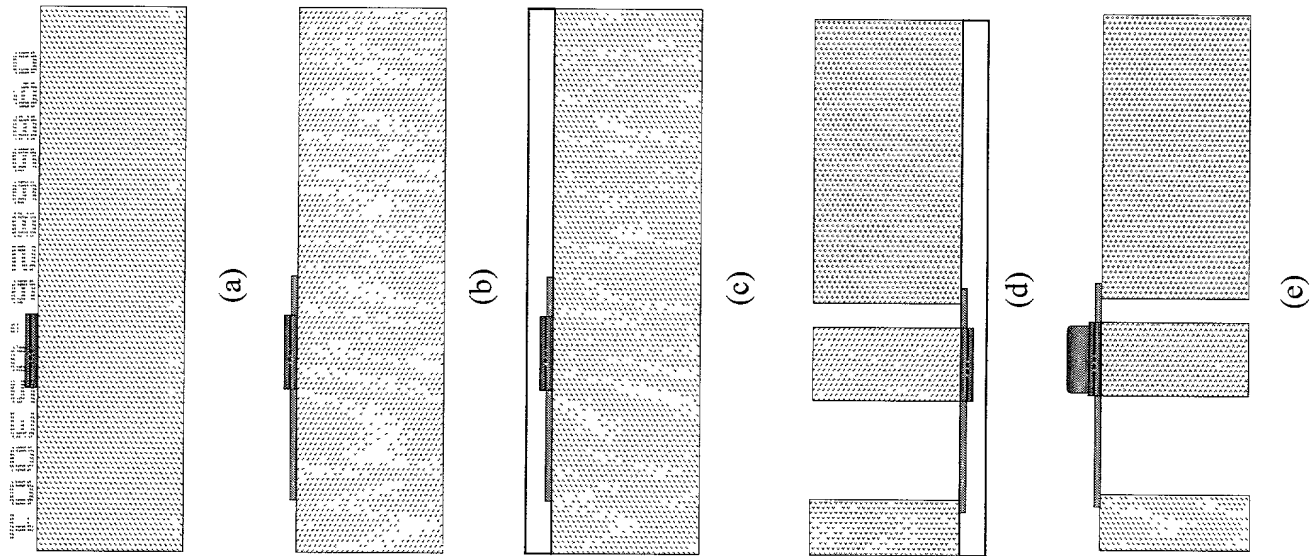


Figure 21

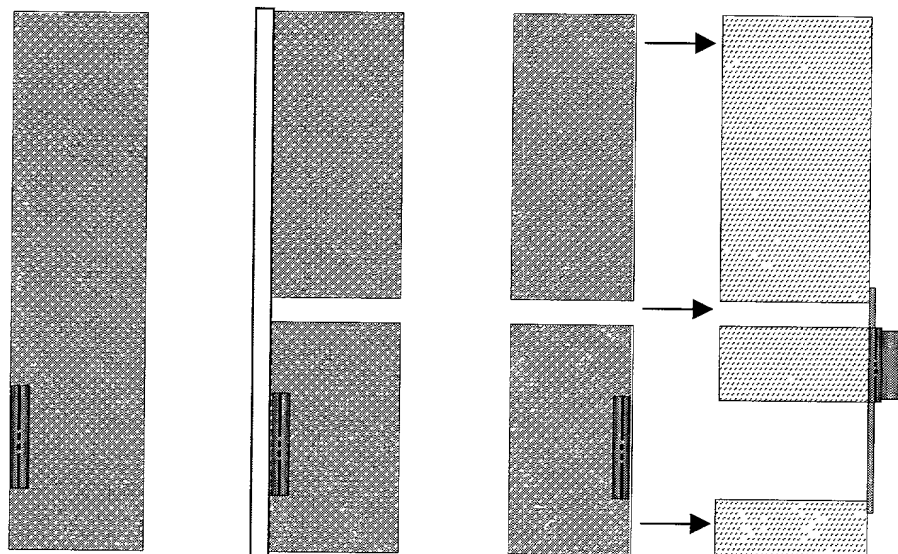


Figure 22

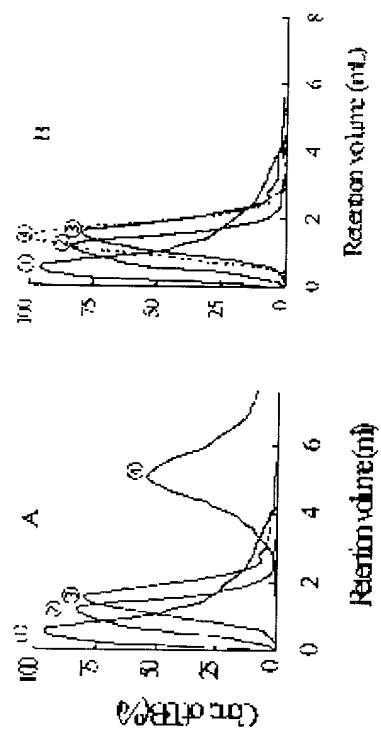


Figure 23

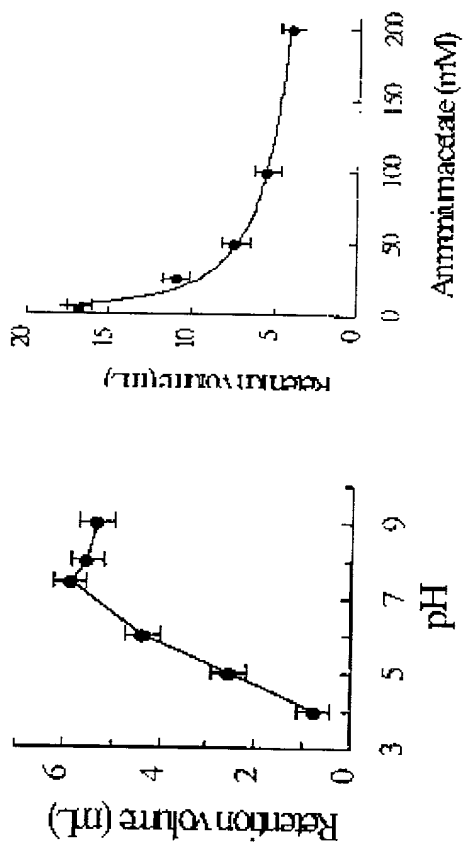


Fig. 3

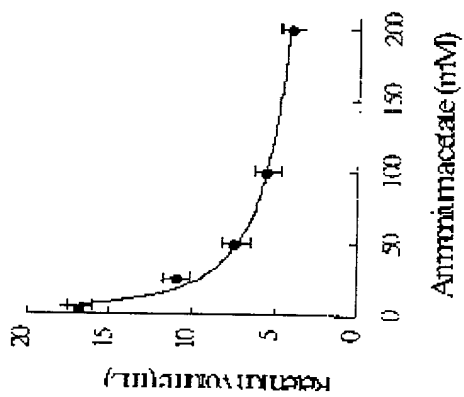


Fig. 4

Figure 24